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What is claimed is:

1. A complementary MOS semiconductor device having an N-channel MOS transistor, a P-channel MOS transistor and a resistor, wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity type of a gate electrode of the P-channel MOS transistor is P-type.

2. A complementary MOS semiconductor device according to claim 1, wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each comprise a single layer of first polycrystalline silicon having a film thickness in a range of 2000 Å to 6000 Å and including boron or BF_2 with an impurity concentration of 1×10^{19} atoms/cm^3 or more.

3. A complementary MOS semiconductor device according to claim 1, wherein the P-type gate electrode of the N-channel MOS transistor and the P-type gate electrode of the P-channel MOS transistor each have a polycide structure comprising a lamination of first polycrystalline silicon having a film thickness in a range of 1000 Å to 4000 Å and including boron or BF_2 with an impurity concentration of 1×10^{19} atoms/cm^3 or more and first high melting point metal silicide selected from the group consisting of molybdenum silicide, tungsten silicide, titanium silicide, and platinum silicide, with a film thickness in a range of 500 Å to 2500 Å.

4. A complementary MOS semiconductor device according to claim 1, wherein the resistor is polycrystalline silicon

formed in the same layer and has the same film thickness range as the first polycrystalline silicon constituting the gate electrode.

5. A complementary MOS semiconductor device according to claim 1, wherein the resistor is second polycrystalline silicon having a film thickness in a range of 500 Å to 2000 Å.

6. A complementary MOS semiconductor device according to claim 1, wherein the resistor is a thin film metal transistor formed from one selected from the group consisting of Ni-Cr alloy, Cr-SiO alloy, molybdenum silicide, and β-ferrite silicde and has a film thickness in a range of 100 Å to 300 Å.

7. A complementary MOS semiconductor device according to claim 1, wherein the resistor comprising the first or the second polycrystalline silicon contains phosphorous or arsenic with an impurity concentration of 1×10^{14} to 9×10^{18} atoms/cm^3 and includes a first N-type transistor of a relatively low concentration having a sheet resistance in an order of several kΩ/square to several tens of kΩ/square.

8. A complementary MOS semiconductor device according to claim 1, wherein the resistor comprising the first or the second polycrystalline silicon contains phosphorous or arsenic with an impurity concentration of 1×10^{19} atoms/cm^3 or more and includes a second N-type transistor of a relatively high concentration having a sheet resistance in an order of about 100 Ω/square to several hundreds of Ω/square and a temperature

coefficient in an order of several hundreds of ppm/°C to about 1000 ppm/°C.

9. A complementary MOS semiconductor device according to claim 1, wherein the resistor comprising the first or the second polycrystalline silicon contains boron or BF_2 with an impurity concentration of 1×10^{14} to 9×10^{18} atoms/cm^3 and includes a first P-type transistor of a relatively low concentration having a sheet resistance in an order of several kΩ/square to several tens of kΩ/square.

10. A complementary MOS semiconductor device according to claim 1, wherein the resistor comprising the first or the second polycrystalline silicon contains boron or BF_2 with an impurity concentration of 1×10^{19} atoms/cm^3 or more and includes a second P-type transistor of a relatively high concentration having a sheet resistance in an order of several hundreds of Ω/square to about 1 kΩ/square and a temperature coefficient in an order of several hundreds of ppm/°C to about 1000 ppm/°C.

11. A complementary MOS semiconductor device according to claim 1, wherein the N-channel MOS transistor and the P-channel MOS transistor include a MOS transistor having a first structure of a single drain structure comprising a diffusion layer with a high impurity concentration in which a source and a drain overlap the P-type gate electrode in a planar manner.

12. A complementary MOS semiconductor device according to

claim 1, wherein the N-channel MOS transistor and the P-channel MOS transistor include a MOS transistor having a second structure comprising a diffusion layer with a low impurity concentration in which only the drain side thereof overlaps the P-type gate electrode in a planar manner or both the source and drain sides thereof overlap the P-type gate electrode in the planar manner and a diffusion layer with a high impurity concentration in which only the drain side thereof does not overlap the P-type gate electrode in the planar manner or both the source and drain sides thereof do not overlap the P-type gate electrode in the planar manner.

13. A complementary MOS semiconductor device according to claim 1, wherein the N-channel MOS transistor and the P-channel MOS transistor include a MOS transistor having a third structure comprising a diffusion layer with a low impurity concentration in which only the drain side thereof overlaps the P-type gate electrode in a planar manner or both the source and drain side thereof overlap the P-type gate electrode in the planar manner and a diffusion layer with a high impurity concentration in which only the drain side thereof does not overlap the P-type gate electrode in the planar manner or both the source and drain sides thereof do not overlap the P-type gate electrode in the planar manner, and an insulating film between the diffusion layer with a high impurity concentration and the P-type gate electrode has

a film thickness thicker than that of a gate insulating film.

14. A complementary MOS semiconductor device according to claim 1, wherein the N-channel MOS transistor and the P-channel MOS transistor include a MOS transistor having a fourth structure comprising a diffusion layer with a high impurity concentration in which both the source and the drain overlap the P-type gate electrode in a planar manner and a diffusion layer with a low impurity concentration in which only the drain side thereof or both the source and drain sides thereof diffuse further on the channel side to overlap the P-type gate electrode in the planar manner.

15. A complementary MOS semiconductor device according to claim 1, wherein, in the N-channel MOS transistor, a channel in which a threshold voltage is in enhancement is a buried channel.

16. A complementary MOS semiconductor device according to claim 1, wherein, in the P-channel MOS transistor, a channel in which a threshold voltage is in enhancement is a surface channel.

17. A complementary MOS semiconductor device according to claim 1, wherein the low impurity concentration diffusion layers in the second structure MOS transistor, the third structure MOS transistor and the fourth structure MOS transistor use arsenic or phosphorous as an impurity with an impurity

concentration of 1×10^{16} to 1×10^{18} atoms/cm^3 in the N-channel MOS transistor and use boron or BF_2 as the impurity with an impurity concentration of 1×10^{16} to 1×10^{18} atoms/cm^3 in the P-channel MOS transistor, and the high impurity concentration diffusion layers in the first structure MOS transistor, the second structure MOS transistor, the third structure MOS transistor and the fourth structure MOS transistor use arsenic or phosphorous as the impurity with an impurity concentration of 1×10^{16} to 1×10^{18} atoms/cm^3 or more in the N-channel MOS transistor and uses boron or BF_2 as the impurity with an impurity concentration of 1×10^{16} to 1×10^{18} atoms/cm^3 or more in the P-channel MOS transistor.

18. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film to form a first N-type region in the first polycrystalline silicon film;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a second P-type region in the first polycrystalline silicon film;

forming a first insulating film on the first polycrystalline silicon film;

patterning the first insulating film and the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first P-type polycrystalline silicon region and a resistor formed from the first N-type polycrystalline silicon region and the second P-type polycrystalline silicon region;

selectively removing the first insulating film on the resistor;

doping a high concentration N-type impurity into regions that become a source and a drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type polycrystalline silicon region; and

doping a high concentration P-type impurity into regions that become a source and a drain of the P-channel MOS transistor and

a part or an entire region of the resistor formed from the second P-type polycrystalline silicon region.

19. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a first P-type region of a first polycrystalline silicon film;

forming a high melting point metal silicide film on the first polycrystalline silicon film;

forming a first insulating film on the high melting point metal silicide film;

patterning the first insulating film, the high melting point metal silicide film and the first polycrystalline silicon film of

the first P-type region to form a gate electrode and a wiring;

forming a fourth insulating film on the semiconductor substrate;

forming a second polycrystalline silicon film on the fourth insulating film;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type region in the second polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type region in the second polycrystalline silicon film;

patterning the second polycrystalline silicon film to form a resistor;

doping a high concentration N-type impurity into regions that become a source and a drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type polycrystalline silicon region; and

doping a high concentration P-type impurity into regions that become a source and a drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type polycrystalline silicon region.

20. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a first P-type region of a first polycrystalline silicon film;

forming a high melting point metal film on the first polycrystalline silicon film;

performing heat treatment for the high melting point metal film, which contacts to the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

forming a first insulating film on the high melting point metal silicide film;

patterning the first insulating film, the high melting point metal silicide film and the first polycrystalline silicon film of the first P-type region to form a gate electrode and a wiring;

forming a fourth insulating film on the semiconductor

substrate;

forming a second polycrystalline silicon film on the fourth insulating film;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type region in the second polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type region in the second polycrystalline silicon film;

patterning the second polycrystalline silicon film to form a resistor;

doping a high concentration N-type impurity into regions that become a source and a drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type polycrystalline silicon region; and

doping a high concentration P-type impurity into regions that become a source and a drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type polycrystalline silicon region.

21. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1 , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor

substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film to form a first N-type region in the first polycrystalline silicon film;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a second P-type region in the first polycrystalline silicon film;

forming a first insulating film on the first polycrystalline silicon film;

patterning the first insulating film and the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first P-type polycrystalline silicon region and a resistor formed from the first N-type polycrystalline silicon region and the second P-type polycrystalline silicon region;

selectively doping a low concentration N-type impurity into regions that become a source and a drain of the N-channel MOS transistor in the semiconductor substrate; and

doping a low concentration P-type impurity into regions that become a source and a drain of the P-channel MOS transistor in the semiconductor substrate;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form a side spacer on a side wall of the first polycrystalline silicon film;

selectively removing the first insulating film on the resistor;

doping a high concentration N-type impurity into regions that become a source and a drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon; and

doping a high concentration P-type impurity into regions that become a source and a drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon.

22. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a first insulating film on the first polycrystalline silicon film;

patterning the first insulating film and the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first P-type polycrystalline silicon region and a resistor region formed from the region other than the first P-type polycrystalline silicon film region;

selectively removing the first insulating film on the resistor region;

selectively doping a low concentration N-type impurity into regions that become a source and a drain of the N-channel MOS

transistor and into the polycrystalline silicon film other than the first P-type polycrystalline silicon film region to form a low concentration N-type source and drain and a first N-type region in the first polycrystalline silicon film;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and into the first polycrystalline silicon film other than the first P-type polycrystalline silicon film region and the first N-type polycrystalline silicon film region to form a low concentration P-type source and drain and a second P-type region in the first polycrystalline silicon film;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form a side spacer on a side wall of the first polycrystalline silicon film;

doping a high concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon; and

doping a high concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon.

23. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region;

forming a first insulating film on the first polycrystalline silicon film;

patterning the first insulating film and the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first polycrystalline silicon region;

selectively doping a low concentration N-type impurity into regions that become a source and a drain of the N-channel MOS transistor in the semiconductor substrate;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor in the semiconductor device;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form a side spacer on a side wall of the first polycrystalline silicon film;

forming a second polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type impurity region;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type polycrystalline silicon region;

patterning the second polycrystalline silicon film to form a resistor;

selectively doping a high concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon; and

selectively doping a high concentration P-type impurity into

regions that become the source and the drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon.

24. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film to form a first N-type polycrystalline silicon region;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region;

doping a low concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a second

P-type polycrystalline silicon region;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first P-type region of the first polycrystalline silicon film;

forming a high melting point metal silicide film on the semiconductor substrate;

selectively removing the high melting point metal silicide film on the patterned second insulating film and in the vicinity thereof;

removing the patterned second insulating film;

forming a first insulating film on the high melting point metal silicide film and the first polycrystalline silicon film;

patterning the first insulating film, the first polycrystalline silicon film and the high melting point metal silicide film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor formed from the first N-type region and the second P-type region of the first polycrystalline silicon film;

selectively doping a low concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor in the semiconductor substrate;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor in the semiconductor substrate;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form side spacers on side walls of the first polycrystalline silicon film and the high melting point metal silicide film;

selectively removing the first insulating film on the resistor;

doping a high concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type polycrystalline silicon region; and

doping a high concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type polycrystalline silicon region.

25. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first P-type region of the first polycrystalline silicon film;

forming a high melting point metal silicide film on the semiconductor substrate;

selectively removing the high melting point metal silicide film on the patterned second insulating film and in the vicinity thereof;

removing the patterned second insulating film;

forming a first insulating film on the high melting point metal silicide film and the first polycrystalline silicon film;

patterning the first insulating film, the first polycrystalline silicon film and the high melting point metal

silicide film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor region formed from the region other than the first P-type region of the first polycrystalline silicon film;

selectively removing the first insulating film on the resistor region;

selectively doping a low concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and the first polycrystalline silicon film other than the first P-type region to form a low concentration N-type source and drain and a first N-type region in the first polycrystalline silicon film;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and the first polycrystalline silicon film other than the first P-type region and the first N-type region to form a low concentration P-type source and drain and a second P-type region in the first polycrystalline silicon film;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form side spacers on side walls of the first polycrystalline

silicon film and the high melting point metal silicide film;

doping a high concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type polycrystalline silicon region; and

doping a high concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type polycrystalline silicon region.

26. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film to form a first N-type

polycrystalline silicon region;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region;

doping a low concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a second P-type polycrystalline silicon region;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first P-type region of the first polycrystalline silicon film;

forming a high melting point metal silicide film on the semiconductor substrate;

performing heat treatment for the high melting point metal film, which contacts to the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

selectively removing non-reacted high melting point metal silicide film on the second insulating film;

removing the patterned second insulating film;

forming a first insulating film on the high melting point metal silicide film and the first polycrystalline silicon film;

patterning the first insulating film, the first polycrystalline silicon film and the high melting point metal silicide film to form a gate electrode and a wiring formed from

a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor formed from the first N-type region and the second P-type region of the first polycrystalline silicon film;

selectively doping a low concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor in the semiconductor substrate;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor in the semiconductor substrate;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form side spacers on side walls of the first polycrystalline silicon film and the high melting point metal silicide film;

selectively removing the first insulating film on the resistor;

doping a high concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type polycrystalline silicon region; and

doping a high concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor

and a part or an entire region of the resistor formed from the second P-type polycrystalline silicon region.

27. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first P-type region of the first polycrystalline silicon film;

forming a high melting point metal silicide film on the semiconductor substrate;

performing heat treatment for the high melting point metal film, which contacts to the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

selectively removing non-reacted high melting point metal silicide film on the second insulating film;

removing the patterned second insulating film;

forming a first insulating film on the high melting point metal silicide film and the first polycrystalline silicon film;

patterning the first insulating film, the first polycrystalline silicon film and the high melting point metal silicide film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor region formed from the region other than the first P-type region of the first polycrystalline silicon film;

selectively removing the first insulating film on the resistor region;

selectively doping a low concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and the first polycrystalline silicon film other than the first P-type region to form a low concentration N-type source and drain and a first N-type region in the first polycrystalline silicon film;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and the first polycrystalline silicon film other than the first P-type region and the first N-type region to form a low concentration P-type source and drain and a second P-type region in the first polycrystalline silicon film;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form side spacers on side walls of the first polycrystalline silicon film and the high melting point metal silicide film;

doping a high concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type polycrystalline silicon region; and

doping a high concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type polycrystalline silicon region.

28. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor

substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a high melting point metal silicide film on the first polycrystalline silicon film;

forming a first insulating film on the high melting point metal silicide film;

patterning the first insulating film, the high melting point metal silicide film and the first polycrystalline silicon film of the first P-type region to form a gate electrode and a wiring;

selectively doping a low concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor in the semiconductor substrate;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor in the semiconductor substrate;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form side spacers on side walls of the first polycrystalline silicon film and the high melting point metal silicide film;

forming a second polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type polycrystalline silicon region;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type polycrystalline silicon region;

patterning the second polycrystalline silicon film to form a resistor;

selectively doping a high concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon region; and

selectively doping a high concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon.

29. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a high melting point metal film on the first polycrystalline silicon film;

performing heat-treatment for the high melting point metal film, which contacts to the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

forming a first insulating film on the high melting point metal silicide film;

patterning the first insulating film, the high melting point

metal silicide film and the first polycrystalline silicon to form a gate electrode and a wiring;

selectively doping a low concentration N-type impurity into regions that become the source and the drain of the N-channel MOS transistor in the semiconductor substrate;

selectively doping a low concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor in the semiconductor substrate;

depositing a third insulating film on the semiconductor substrate;

etching the third insulating film by anisotropic dry etching to form side spacers on side walls of the first polycrystalline silicon film and the high melting point metal silicide film;

forming a second polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type polycrystalline silicon region;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type polycrystalline silicon region;

patterning the second polycrystalline silicon film to form a resistor;

selectively doping a high concentration N-type impurity into

regions that become the source and the drain of the N-channel MOS transistor and a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon region; and

selectively doping a high concentration P-type impurity into regions that become the source and the drain of the P-channel MOS transistor and a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon.

30. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film to form a first N-type polycrystalline silicon region;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region in the first polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a second P-type polycrystalline silicon region in the first polycrystalline silicon film;

patterning the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first P-type region of the first polycrystalline silicon film and a resistor formed from the first N-type region and the second P-type region of the first polycrystalline silicon film;

doping a low concentration N-type impurity into the semiconductor substrate so that a source and a drain overlap a gate electrode of the N-channel MOS transistor in a planar manner

selectively doping a low concentration P-type impurity into the semiconductor substrate so that both a source and a drain or only the drain side thereof overlap a gate electrode of the P-channel MOS transistor in the planar manner;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the

N-channel MOS transistor in a planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

31. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type

polycrystalline silicon region in the first polycrystalline silicon film;

patterning the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first P-type region of the first polycrystalline silicon film and a resistor formed from the region other than the first P-type region of the first polycrystalline silicon film;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film other than the semiconductor substrate and the first P-type region where the source and the drain overlap the gate electrode of the N-channel MOS transistor in a planer manner to form first N-type regions in the low concentration N-type source and drain and the first polycrystalline silicon film;

selectively doping a low concentration P-type impurity into the first polycrystalline silicon film other than the semiconductor substrate, the first P-type region and the second N-type region where both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-channel MOS transistor in a planer manner to form second P-type regions in the low concentration source and drain or only drain of the P-channel MOS transistor and the first polycrystalline silicon film;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon film and the

source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in a planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

32. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into the first

polycrystalline silicon film to form a first P-type polycrystalline silicon region in the first polycrystalline silicon film;

patterning the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first P-type region;

forming a fourth insulating film on the semiconductor substrate;

forming a second polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type region in the second polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type region in the second polycrystalline silicon film;

patterning the second polycrystalline silicon film to form a resistor;

doping a low concentration N-type impurity into the semiconductor substrate so that the source and the drain overlap the gate electrode of the N-channel MOS transistor in a planar manner;

doping a low concentration P-type impurity into the semiconductor substrate so that both the source and the drain or only the drain side thereof overlap the gate electrode of the P-channel MOS transistor in the planar manner;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in a planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

33. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, ..., comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region in the first polycrystalline silicon film;

patterning the first polycrystalline silicon film to form a gate electrode and a wiring formed from the first P-type region;

forming a fourth insulating film on the semiconductor substrate;

forming a second polycrystalline silicon film on the semiconductor substrate;

patterning the second polycrystalline silicon film to form a resistor;

selectively doping a low concentration N-type impurity into the region where source and the drain overlap the gate electrode of the N-channel MOS transistor in a planer manner and the second polycrystalline silicon film to simultaneously form first N-type regions in the low concentration source and drain of the N-channel MOS transistor and the second polycrystalline silicon film;

selectively doping a low concentration P-type impurity into the region where both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-channel MOS transistor in a planer manner and the second polycrystalline silicon film to simultaneously form second P-type regions in the low

concentration source and drain or drain of the P-channel MOS transistor and the second polycrystalline silicon film;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in a planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in a planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

34. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film to form a first N-type polycrystalline silicon region in the first polycrystalline silicon film;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region in the first polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a second P-type polycrystalline silicon region in the first polycrystalline silicon film;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first P-type region of the first polycrystalline silicon film;

forming a high melting point metal silicide film on the semiconductor substrate;

selectively removing the high melting point silicide film on the patterned second insulating film and in the vicinity thereof;

removing the patterned second insulating film;

patterning the first polycrystalline silicon film and the high melting point metal silicide film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor region formed from the first N-type region of the first polycrystalline silicon film and the second P-type region;

doping a low concentration N-type impurity into the semiconductor substrate so that the source and the drain overlap the gate electrode of the N-channel type MOS transistor in the planar manner;

doping a low concentration P-type impurity into the semiconductor substrate so that both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-type MOS transistor in the planar manner;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon film and the

region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in a planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

35. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first

P-type region of the first polycrystalline silicon film;

forming a high melting point metal silicide film on the semiconductor substrate;

selectively removing the high melting point silicide film on the patterned second insulating film and in the vicinity thereof;

removing the patterned second insulating film;

patterning the first polycrystalline silicon film and the high melting point metal silicide film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor region formed from the region other than the first P-type region of the first polycrystalline silicon film;

selectively doping a low concentration N-type impurity into the region where the source and the drain overlap the gate electrode of the N-channel MOS transistor in a planer manner and the first polycrystalline silicon film other than the first P-type region to simultaneously form first N-type regions in the low concentration source and drain of the N-channel MOS transistor and the first polycrystalline silicon film;

selectively doping a low concentration P-type impurity into the region where both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-channel MOS transistor in a planer manner and the first polycrystalline silicon

film other than the first P-type region and the first N-type region to simultaneously form second P-type regions in the low concentration source and drain or only drain of the P-channel MOS transistor and the first polycrystalline silicon film;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in a planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

36. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor

substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the first polycrystalline silicon film to form a first N-type region in the first polycrystalline silicon film;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type polycrystalline silicon region in the first polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a second P-type polycrystalline silicon region in the first polycrystalline silicon film;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first P-type region of the first polycrystalline silicon film;

forming a high melting point metal film on the semiconductor substrate;

performing heat treatment for the high melting point metal

film, which contacts to the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

selectively removing non-reacted high melting point film on the second insulating film;

removing the patterned second insulating film;

patterning the first polycrystalline silicon film and the high melting point metal film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor region formed from the first N-type region of the first polycrystalline silicon film and the second P-type region;

doping a low concentration N-type impurity into the semiconductor substrate so that the source and the drain overlap the gate electrode of the N-channel type MOS transistor in the planar manner;

doping a low concentration P-type impurity into the semiconductor substrate so that both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-type MOS transistor in the planar manner;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the

N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in a planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

37. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

selectively doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region

in the first polycrystalline silicon film;

forming a second insulating film on the first polycrystalline silicon film;

selectively removing the second insulating film on the first P-type region of the first polycrystalline silicon film;

forming a high melting point metal film on the semiconductor substrate;

performing heat treatment for the high melting point metal film, which contacts to the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

selectively removing non-reacted high melting point film on the second insulating film;

removing the patterned second insulating film;

patterning the first polycrystalline silicon film and the high melting point metal silicide film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film and a resistor region formed from the region other than the first P-type region of the first polycrystalline silicon film;

selectively doping a low concentration N-type impurity into the region where the source and the drain overlap the gate electrode of the N-channel MOS transistor in a planer manner and the first polycrystalline silicon film other than the first P-type region

to simultaneously form first N-type regions in the low concentration source and drain of the N-channel MOS transistor and the first polycrystalline silicon film;

selectively doping a low concentration P-type impurity into the region where both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-channel MOS transistor in a planer manner and the first polycrystalline silicon film other than the first P-type region and the first N-type region to simultaneously form second P-type regions in the low concentration source and drain or only drain of the P-channel MOS transistor and the first polycrystalline silicon film;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the first polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the first polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in a planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

38. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a high melting point metal silicide film on the first polycrystalline silicon film;

patterning the high melting point metal silicide film and the first polycrystalline silicon film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film;

forming a fourth insulating film on the semiconductor

substrate;

forming a second polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type region in the second polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type region in the second polycrystalline silicon film;

patterning the second polycrystalline silicon film to form a resistor;

doping a low concentration N-type impurity into the semiconductor substrate so that a source and a drain overlap a gate electrode of the N-channel MOS transistor in the planar manner;

selectively doping a low concentration P-type impurity into the semiconductor substrate so that both a source and a drain or only the drain side thereof overlaps a gate electrode of the P-channel MOS transistor in the planar manner;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into

a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

39. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a high melting point metal silicide film on the first

polycrystalline silicon film;

patterning the high melting point metal silicide film and the first polycrystalline silicon film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film;

forming a fourth insulating film on the semiconductor substrate;

forming a second polycrystalline silicon film on the semiconductor substrate;

patterning the second polycrystalline silicon film to form a resistor;

selectively doping a low concentration N-type impurity into the region where the source and the drain overlap the gate electrode of the N-channel MOS transistor in a planer manner and the second polycrystalline silicon film to simultaneously form first N-type regions in the low concentration source and drain of the N-channel MOS transistor and the second polycrystalline silicon film;

selectively doping a low concentration P-type impurity into the region where both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-channel MOS transistor in a planer manner and the second polycrystalline silicon film to simultaneously form second P-type regions in the low concentration source and drain or the drain of the P-channel MOS

transistor and the second polycrystalline silicon film;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

40. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1 , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the

semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a high melting point metal film on the first polycrystalline silicon film;

performing heat treatment for the high melting point metal film, which contacts the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

patterning the high melting point metal silicide film and the first polycrystalline silicon film to form a gate electrode and a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film;

forming a fourth insulating film on the semiconductor substrate;

forming a second polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form the first N-type region in the second polycrystalline silicon film;

doping a low concentration P-type impurity into an entire

region of the second polycrystalline silicon film to form a second P-type region in the second polycrystalline silicon film;

patterning the second polycrystalline silicon film to form a resistor;

doping a low concentration N-type impurity into the semiconductor substrate so that the source and the drain overlap the gate electrode of the N-channel MOS transistor in a planar manner;

doping a low concentration P-type impurity into the semiconductor substrate so that both the source and the drain or the drain overlaps the gate electrode of the P-channel MOS transistor in the planar manner;

selectively doping a high concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap

the gate electrode in the planar manner.

41. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, , comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a high melting point metal film on the first polycrystalline silicon film;

performing heat treatment for the high melting point metal film, which contacts the first polycrystalline silicon film, to obtain a high melting point metal silicide film;

patterning the high melting point metal silicide film and the first polycrystalline silicon film to form a gate electrode and

a wiring formed from a lamination layer of the first P-type region of the first polycrystalline silicon film and the high melting point metal silicide film;

forming a fourth insulating film on the semiconductor substrate;

forming a second polycrystalline silicon film on the semiconductor substrate;

patterning the second polycrystalline silicon film to form a resistor;

selectively doping a low concentration N-type impurity into the region where source and the drain overlap the gate electrode of the N-channel MOS transistor in a planer manner and the second polycrystalline silicon film to simultaneously form first N-type regions in the low concentration source and drain of the N-channel MOS transistor and the second polycrystalline silicon film;

selectively doping a low concentration P-type impurity into the region where both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-channel MOS transistor in a planer manner and the second polycrystalline silicon film to simultaneously form second P-type regions in the low concentration source and drain or drain of the P-channel MOS transistor and the second polycrystalline silicon film;

selectively doping a low concentration N-type impurity into a part or an entire region of the resistor formed from the first

N-type region of the second polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

42. A method of manufacturing a complementary MOS semiconductor device as claimed in claim 1, comprising the steps of:

forming wells for defining respective regions of an N-channel MOS transistor and a P-channel MOS transistor in a semiconductor substrate;

forming an element isolating region on the semiconductor substrate;

forming a gate insulating film on the semiconductor substrate;

doping an impurity for controlling a threshold value into the semiconductor substrate;

forming a first polycrystalline silicon film on the semiconductor substrate;

doping a high concentration P-type impurity into an entire region of the first polycrystalline silicon film to form a first P-type region in the first polycrystalline silicon film;

forming a high melting point metal silicide film on the first polycrystalline silicon film;

forming a first insulating film on th high melting point metal silicide film;

patterning the first insulating film, the high melting point metal silicide film and the first polycrystalline silicon film to form a gate electrode and a wiring;

forming a fourth insulating film on the semiconductor substrate;

forming a second polycrystalline silicon film on the semiconductor substrate;

selectively doping a low concentration N-type impurity into the second polycrystalline silicon film to form a first N-type region in the second polycrystalline silicon film;

doping a low concentration P-type impurity into an entire region of the second polycrystalline silicon film to form a second P-type region in the second polycrystalline silicon film;

patterning the second polycrystalline silicon film to form a resistor;

selectively doping a low concentration N-type impurity into the semiconductor substrate so that both a source and a drain or

only the drain side thereof overlaps the gate electrode of the N-channel MOS transistor in a planar manner;

selectively doping a low concentration P-type impurity into the semiconductor substrate so that both the source and the drain or only the drain side thereof overlaps the gate electrode of the P-channel MOS transistor in the planar manner;

selectively doping a low concentration N-type impurity into a part or an entire region of the resistor formed from the first N-type region of the second polycrystalline silicon film and the source and drain regions not overlapping the gate electrode of the N-channel MOS transistor in the planer manner, or the region where the source side thereof overlaps the gate electrode in a planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner; and

selectively doping high concentration P-type impurities into a part or an entire region of the resistor formed from the second P-type region of the second polycrystalline silicon film and the region where both the source and the drain do not overlap the gate electrode of the P-channel MOS transistor in a planer manner or the region where the source side thereof overlaps the gate electrode in the planar manner and only the drain side thereof does not overlap the gate electrode in the planar manner.

43. A complementary MOS semiconductor device according to claim 1, , wherein the semiconductor

substrate is a P-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming an N-type well, respectively.

44. A complementary MOS semiconductor device according to claim 1, wherein the semiconductor substrate is a P-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming an N-type well and a P-type well, respectively.

45. A complementary MOS semiconductor device according to claim 1, wherein the semiconductor substrate is an N-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming a P-type well, respectively.

46. A complementary MOS semiconductor device according to claim 1, wherein the semiconductor substrate is an N-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming an N-type well and a P-type well, respectively.

47. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the semiconductor substrate is a P-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming an N-type well, respectively.

48. A method of manufacturing a complementary MOS

semiconductor device according to claim 18, wherein the semiconductor substrate is a P-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming an N-type well and a P-type well, respectively.

49. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the semiconductor substrate is an N-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming a P-type well, respectively.

50. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the semiconductor substrate is an N-type semiconductor substrate, and regions of the N-channel MOS transistor and the P-channel MOS transistor are defined by forming an N-type well and a P-type well, respectively.

51. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the step of forming the element isolating region on the semiconductor substrate is performed by a LOCOS method.

52. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the step of forming the element isolating region on the semiconductor substrate is performed by a shallow trench isolation method.

53. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the step of doping impurities for the threshold control is performed by an ion injection method, and the impurity for the threshold control of the N-channel MOS transistor is arsenic or phosphorous.

54. A complementary MOS semiconductor device according to claim 1, wherein the first polycrystalline silicon is formed by a chemical vapor deposition method.

55. A complementary MOS semiconductor device according to claim 1, wherein the second polycrystalline silicon is formed by a chemical vapor deposition method or a sputtering method.

56. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the first polycrystalline silicon is formed by a chemical vapor deposition method.

57. A method of manufacturing a complementary MOS semiconductor device according to claim 19, wherein the second polycrystalline silicon is formed by a chemical vapor deposition method or a sputtering method.

58. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the first P-type region of the first polycrystalline silicon is formed by an ion injection method using boron or BF_2 as impurities, a

pre-deposition and drive-in method in an electric furnace using boron as an impurity or a molecular layer doping method using boron as the impurity.

59. A method of manufacturing a complementary MOS semiconductor device according to claim 19, wherein the step of forming the first P-type region of the first polycrystalline silicon is performed by a chemical vapor deposition method for depositing polycrystalline silicon and simultaneously doping boron as an impurity.

60. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the first insulating film is a silicon oxide film formed by a chemical vapor deposition method or a thermal oxidization method and has a film thickness in a range of 1000 Å to 2000 Å.

61. A method of manufacturing a complementary MOS semiconductor device according to claim 18, wherein the first insulating film is a silicon oxide film formed by a chemical vapor deposition method and has a film thickness in a range of 1000 Å to 2000 Å.

62. A method of manufacturing a complementary MOS semiconductor device according to claim 21, wherein a lower layer of the first insulating film is a silicon oxide film formed by a chemical vapor deposition method or a thermal

oxidization method; an upper layer thereof is formed by the chemical vapor deposition method; and a total film thickness of the first insulating is in a range of 1000 Å to 3000 Å.

63. A method of manufacturing a complementary MOS semiconductor device according to claim 24, wherein the second insulating film is formed by a chemical vapor deposition method and has a film thickness in a range of 1000 Å to 4000 Å.

64. A method of manufacturing a complementary MOS semiconductor device according to claim 21, wherein the third insulating film is a silicon oxide film formed by a chemical vapor deposition method and has a total film thickness in a range of 2000 Å to 6000 Å.

65. A complementary MOS semiconductor device according to claim 1, wherein the high melting point metal silicide is formed by a chemical vapor deposition method or a sputtering method.

66. A method of manufacturing a complementary MOS semiconductor device according to claim 19, wherein the high melting point metal silicide is formed by a chemical vapor deposition method or a sputtering method.

67. A method of manufacturing a complementary MOS semiconductor device according to claim 20, wherein the high melting point metal is cobalt or titanium

formed by a sputtering method and has a film thickness in a range of 100 Å to 500 Å.

68. A semiconductor device, wherein, in a reference voltage circuit in which a gate and a drain of an enhancement NMOS transistor in which the gate and the drain are short-circuited, are connected to a gate and a source of a depletion NMOS transistor in which the gate and the source are short-circuited, and the connection node is used as an output node, the polarities of gate electrodes of the enhancement NMOS transistor and the depletion NMOS transistor are a P-type.

69. A semiconductor device, wherein, in a reference voltage circuit in which a source of an enhancement NMOS transistor in which the gate and the drain are short-circuited, is connected to a drain of a depletion NMOS transistor in which the gate and the source are short-circuited, and the connection node is used as an output node, the polarities of gate electrodes of the enhancement NMOS transistor and the depletion NMOS transistor are a P-type.

70. A semiconductor device, wherein, in a reference voltage circuit in which a gate and a drain of an enhancement NMOS transistor in which the gate and the drain are short-circuited, are connected to a source of a depletion NMOS transistor in which a gate is short-circuited with a source of the enhancement NMOS transistor and the connection node is used as an output node, the polarities of gate electrodes of the enhancement NMOS transistor and the

depletion NMOS transistor are a P-type.

71. A semiconductor device, wherein, in a reference voltage circuit in which: a drain of a depletion NMOS transistor in which a gate and a source are short-circuited is connected to a drain and a gate of a first enhancement PMOS transistor in which a source is connected to a power supply; a drain of a second enhancement PMOS transistor in which a source is connected to a power supply and a gate is connected commonly to the first enhancement PMOS transistor is connected to a gate and a drain of an enhancement NMOS transistor in which the gate and the drain are short-circuited; and the connection node is used as an output node, the polarities of gate electrodes of the enhancement NMOS transistor and the depletion NMOS transistor are a P-type.

72. A semiconductor device, wherein, in a reference voltage circuit in which: a drain of a first depletion NMOS transistor in which a gate and a source are short-circuited, is connected to a gate and a source of a second depletion NMOS transistor in which the gate and the source are short-circuited; a drain of the second depletion NMOS transistor is connected to a power supply; the source of the first depletion NMOS transistor is connected to an enhancement NMOS transistor in which a gate and a drain are short-circuited; and the connection node is used as an output node, the polarities of gate electrodes of the enhancement NMOS transistor, the first depletion NMOS transistor, and the second depletion NMOS

transistor are a P-type.

73. A semiconductor device, wherein, in a reference voltage circuit in which: a gate and a drain of an enhancement NMOS transistor in which the gate and the drain are short-circuited, are connected with a source of a first depletion NMOS transistor in which a gate is connected to a source of the enhancement NMOS transistor; a drain of the first depletion NMOS transistor is connected to a gate and a source of a second depletion NMOS transistor in which the gate and the source are short-circuited; a drain of the second depletion NMOS transistor is connected to a power supply; and the connection node of the drain of the enhancement NMOS transistor and the source of the first depletion NMOS transistor is used as an output node, the polarities of gate electrodes of the enhancement NMOS transistor, the first depletion NMOS transistor, and the second depletion NMOS transistor are a P-type.

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